UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Ex parte MICHAEL FETTERMAN, STEWART GLENN CARLTON,
JACK HILAIRE CHOQUETTE, SHIRISH GADRE, OLIVIER GIROUX,
DOUGLAS J. HAHN, STEVEN JAMES HEINRICH, ERIC LYELL HILL,
CHARLES McCARVER, OMKAR PARANJAPE,
ANJANA RAJENDRAN, and RAJESHWARAN SELVANESAN

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Appeal 2016-007212
Application 13/370,173[1]
Technology Center 2100

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Before DEBRA K. STEPHENS, JOSEPH P. LENTIVECH, and
AARON W. MOORE, *Administrative Patent Judges*.

LENTIVECH, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants seek our review under 35 U.S.C. § 134(a) of the
Examiner's final rejection of claims 1–20, all the claims pending in the
application on appeal. We have jurisdiction over the pending claims under
35 U.S.C. § 6(b).

We affirm.

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[1] According to Appellants, the real party in interest is NVIDIA Corporation.
App. Br. 3.

STATEMENT OF CASE

Appellants' Invention

Appellants' disclosed invention relates to

[A]n optimized way to execute pre-scheduled replay operations for divergent operations in a parallel processing subsystem. Specifically, a streaming multiprocessor (SM) includes a multi-stage pipeline configured to insert pre-scheduled replay operations into a multi-stage pipeline. A pre-scheduled replay unit detects whether the operation associated with the current instruction is accessing a common resource. If the threads are accessing data which are distributed across multiple cache lines, then the pre-scheduled replay unit inserts pre-scheduled replay operations behind the current instruction. The multi-stage pipeline executes the instruction and the associated pre-scheduled replay operations sequentially.

Spec., Abstract. Claim 1, which is illustrative, reads as follows:

1.   A computer-implemented method for pre-scheduling replay of a common resource access operation, the method comprising:

receiving a first instruction that is to be executed by a group of threads in a multistage pipeline;

determining that a pre-scheduled replay operation should be inserted into the multi-stage pipeline to allow a second set of one or more threads from the group of threads to execute the first instruction;

selecting a first set of one or more threads from the group of threads to execute the first instruction in the multi-stage pipeline;

inserting the first instruction into the multi-stage pipeline for execution by the first set of one or more threads; and

inserting the pre-scheduled replay operation into the multi-stage pipeline to allow the second set of one or more threads to execute the first instruction,

> wherein the first set of one or more threads is intended to access a first aspect or portion of a common resource, and the second set of one or more threads is intended to access a second aspect or portion of the common resource.

Rejection

Claims 1–20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Merchant et al. (US 2002/0091914 A1; published July 11, 2002) ("Merchant") and Shebanow (US 2011/0078358 A1; published Mar. 31, 2011). Final Act. 2–6.

Issue on Appeal

Did the Examiner err by finding the combination of Merchant and Shebanow teaches or suggests the limitations recited in claim 1?

ANALYSIS

Appellants contend the combination of Merchant and Shebanow does not teach or suggest

> determining that a pre-scheduled replay operation should be inserted into the multi-stage pipeline to allow a second set of one or more threads from the group of threads to execute the first instruction; [and]
>
> selecting a first set of one or more threads from the group of threads to execute the first instruction in the multi-stage pipeline,

as recited in claim 1. App. Br. 11–15; Reply Br. 3–4. In particular, Appellants contend "Merchant does not teach or suggest determining that a pre-scheduled replay operation should be inserted into the multi-stage pipeline." App. Br. 12. Appellants contend Merchant, instead, teaches "that

the determination to insert the copy of the instruction through the multiplexer is made only <u>after</u> the instruction fails to properly execute in the execution unit." App. Br. 12 (citing Merchant, Fig. 1, ¶¶ 34–38, 43). According to Appellants, the plain meaning of "pre-scheduled" is "scheduled in advance or prearranged" and, therefore, claim 1 requires "that the claimed replay operation is one that has been scheduled in advance or pre-arranged." App. Br. 13 (citing Wiktionary, https://en.wiktionary.org/ wiki/preschedule (last accessed Apr. 19, 2017)). Appellants contend, therefore, that because Merchant teaches that the determination to insert the copy of the instruction through the multiplexer is made only after the instruction fails to properly execute in the execution unit, Merchant fails to teach or suggest "determining that a pre-scheduled replay operation should be inserted into the multi-stage platform," as required by claim 1. App. Br. 13.

We do not find Appellants' contention persuasive. Appellants essentially argue that "pre-scheduled replay operation," as recited in claim 1, requires that the replay operation be scheduled prior to or in advance of the replay operation being inserted into the multi-stage pipeline. *See* App. Br. 13. We disagree. Initially, we note Appellants' proffered definition is not evidence of how an ordinarily skilled artisan would have interpreted "pre-scheduled" *at the time of the invention.* Nevertheless, even if we construe "pre-scheduled" as "scheduled in advance or prearranged," we agree with the Examiner (Ans. 2–3) that neither the definition nor the claim provides any limitation as to what the replay operation must be scheduled or prearranged in advance of. Therefore, Appellants' contention is not commensurate with the scope of claim 1, and thus, for that reason, does not

demonstrate error in the Examiner's rejection of claim 1. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (limitations not appearing in the claims cannot be relied upon for patentability).

Appellants further contend the combination of Merchant and Shebanow fails to teach or suggest the disputed limitations because Merchant fails to teach the claimed first and second sets of threads. App. Br. 14–15; Reply Br. 3–4. Appellants contend "[b]ecause Merchant teaches that the instruction, and by extension, the copy of the instruction, belong to the same thread, Merchant cannot teach or suggest a first instruction for execution by a <u>first</u> set of threads and a replay operation to allow a <u>second</u> set of threads to execute the first instruction, as claim 1 explicitly requires." App. Br. 14 (citing Merchant, Fig. 1, ¶¶ 34–38, 43, 85).

We agree with Appellants (App. Br. 14) that Merchant teaches execution of an instruction and a copy of the instruction (e.g., a replay operation) by the same thread (*see* Merchant ¶¶ 84–85). However, contrary to Appellants' contention, claim 1 does not prohibit the first set of threads from being the same as the second set of threads or the sets having some of the same threads. Although the Specification describes an example embodiment where a streaming multiprocessor determines that a pre-scheduled replay operation should be inserted into the multi-stage pipeline to allow an *additional* thread to execute the first instruction (Spec., Fig. 5, ¶¶ 73–74), to read a claim in light of the Specification, one must interpret limitations explicitly recited in the claim, without reading limitations from the Specification into the claim that narrow the scope of the claim by implicitly adding disclosed limitations that are not recited in the claim. *In re Prater*, 415 F.2d 1393, 1404–05, (CCPA 1969); *see also In re Van Geuns*,

988 F.2d 1181 (Fed. Cir. 1993). Appellants' contention, therefore, is not commensurate with the scope of claim 1, and thus, for that reason, does not demonstrate error in the Examiner's rejection of claim 1. *See In re Self*, 671 F.2d at 1348.

For the foregoing reasons, we are not persuaded the Examiner erred in rejection claim 1 or claims 2–20, which are not separately argued with particularity.

DECISION

We affirm the Examiner's rejection of claims 1–20 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED